L Number	Hits	Search Text	DB	Time stamp
1	16123	tim$4 near5 constraint	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:01
2	3046	(tim$4 near5 constraint) and (clock near5 signal)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:01
3	61	(((((tim$4 near5 constraint) and (clock near5 signal)) and 716/$.ccls.) and internal and external and test) and static) and relat$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:01
4	39	(((((((tim$4 near5 constraint) and (clock near5 signal)) and 716/$.ccls.) and internal and external and test) and static) and relat$6) and multip$6) and paramet$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:01
5	367	((tim$4 near5 constraint) and (clock near5 signal)) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:01
6	128	(((tim$4 near5 constraint) and (clock near5 signal)) and 716/$.ccls.) and internal and external	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:01
7	86	(((tim$4 near5 constraint) and (clock near5 signal)) and 716/$.ccls.) and internal and external and test	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:04
8	61	((((tim$4 near5 constraint) and (clock near5 signal)) and 716/$.ccls.) and internal and external and test) and static	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:01
9	46	((((((tim$4 near5 constraint) and (clock near5 signal)) and 716/$.ccls.) and internal and external and test) and static) and relat$6) and multip$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:01
10	59	(((tim$4 near5 constraint) and (clock near5 signal)) and 716/$.ccls.) and internal and external and test and (eliminat$4 or delelet$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:05
11	43	(((tim$4 near5 constraint) and (clock near5 signal)) and 716/$.ccls.) and internal and external and test and (eliminat$4 or delelet$4) and parameter	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:05
12	29	(((tim$4 near5 constraint) and (clock near5 signal)) and 716/$.ccls.) and internal and external and test and (eliminat$4 or delelet$4) and parameter and boundar$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/15 07:05

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040025129 A1	20040205	18	System and methods for pre-artwork signal-timing verification of an integrated circuit design	716/6
2	US 20030233622 A1	20031218	84	Method and apparatus for an asynchronous pulse logic circuit	716/1
3	US 20030208723 A1	20031106	68	Automated processor generation system for designing a configurable processor and method for the same	716/1
4	US 20030009727 A1	20030109	90	Circuit designing apparatus, circuit designing method and timing distribution apparatus	716/1
5	US 20020162086 A1	20021031	19	RTL annotation tool for layout induced netlist changes	716/18
6	US 20020083398 A1	20020627	90	Circuit designing apparatus, circuit designing method and timing distribution apparatus	716/1
7	US 6760888 B2	20040706	65	Automated processor generation system for designing a configurable processor and method for the same	716/1
8	US 6732336 B2	20040504	81	Method and apparatus for an asynchronous pulse logic circuit	716/1
9	US 6678871 B2	20040113	84	Circuit designing apparatus, circuit designing method and timing distribution apparatus	716/6
10	US 6618834 B2	20030909	88	Circuit designing apparatus, circuit designing method and timing distribution apparatus	716/2
11	US 6530073 B2	20030304	18	RTL annotation tool for layout induced netlist changes	716/18

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15	US 6295636 B1	20010925	82	RTL analysis for improved logic synthesis	716/18
16	US 6292931 B1	20010918	81	RTL analysis tool	716/18
17	US 6289498 B1	20010911	81	VDHL/Verilog expertise and gate synthesis automation system	716/18
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27	US 5623418 A	19970422	66	System and method for creating and validating structural description of electronic system	716/1
28	US 5555201 A	19960910	95	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	716/1
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Solid-State Circuits, IEEE Journal of , Volume: 24 , Issue: 1 , Feb. 1989
Pages:146 - 157

[Abstract] [PDF Full-Text (860 KB)] **IEEE JNL**

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3 **Clock period optimization in a multiphase edge-clocked circuit constrained to a maximum number of phases**
Fernandez, F.; Sanchez, A.;
EUROMICRO 97. 'New Frontiers of Information Technology'. Short Contributio Proceedings of the 23rd Euromicro Conference , 1-4 Sept. 1997
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[Abstract] [PDF Full-Text (232 KB)] **IEEE CNF**

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